REMARKS

Claims 1-15 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

In the instant Office Action dated March 8, 2007, the following rejections are noted: claims 1-2, 5-6, and 14 stand rejected under 35 U.S.C. 102(b) over Shiga (U.S. Patent No. 6,778,443); claims 3-4 stand rejected under 35 U.S.C. 103(a) over Shiga in view of Yamazoe (U.S. Patent No. 7,009,890); claim 7 stands rejected under 35 U.S.C. 103(a) over Shiga in view of Hirakawa (U.S. Patent Pub. 2001/0007541); and claims 8-13 stand rejected under 35 U.S.C. 103(a) over Shiga in view of Hirakawa and further in view of Yamazoe.

Applicant respectfully traverses that Section 102(b) rejection of claims 1-2, 5-6 and 14 because the cited portions of the Shiga reference do not correspond to the claimed invention which includes, for example, aspects directed to an array of nonvolatile charge trapping memory devices. According to M.P.E.P. § 2111.01(I), the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with Applicant's specification. *See also In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989). In this instance, the Office Action has improperly interpreted the claimed charge trapping memory device as corresponding to a floating gate memory device. Applicant's specification, however, clearly differentiates a charge trapping device from a floating gate device. *See, e.g.,* Paragraph 0003. Thus, the cited portions of the Shiga reference do not teach charge trapping memory devices since Shiga's memory cell has a floating gate. *See, e.g.,* Col. 1:63 to Col. 2:3. Accordingly, the Section 102(b) rejection of claims 1-2, 5-6 and 14 is improper and Applicant requests that it be withdrawn. Applicant notes that the Section 102(b) rejection of claims 1-2, 5-6 and 14 is also improper because the Shiga reference does not qualify as prior art under Section 102(b).

Notwithstanding the above traversal, in an effort to facilitate prosecution, Applicant has amended claims 1 and 5 to clarify that which would have been clear to one of skill in the art. Specifically, that the charge trapping memory devices are charged during programming and that they are discharged during erasing. Applicant submits that

the operation of a charge trapping memory device is different from that of a floating gate drive, which is discharged during the program operation and charged during the erase operation. *See, e.g.,* Paragraph 0006 of Applicant's specification citing U.S. Patent No. 6,233,178. Accordingly, Applicant requests that the Section 102(b) rejection of claims 1-2, 5-6 and 14 be withdrawn.

Applicant further traverses the Section 102(b) rejection of claim 6 because the Office Action's assertion that it is inherent that Shiga's memory cell has a dielectric charge trapping layer is improper. Accordingly to M.P.E.P. § 2112(IV), "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." In this instance, the Shiga reference teaches a memory cell that has a floating gate in which electrons are trapped. *See, e.g.,* Col. 1:63 to Col. 2:3. Thus, Shiga's memory cells do not have a dielectric charge trapping layer as in the claimed invention. Accordingly, the Office Action's assertion of inherency is improper. Therefore, the Section 102(b) rejection of claim 6 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the Section 103(a) rejection of claims 3-4 because the Office Action has provided no evidence of motivation to combine the Shiga and Yamazoe references. This approach is contrary to the requirements of Section 103 and relevant law. "A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007). The Office Action asserts that one of skill in the art would combine the reference cells taught by Yamazoe in the circuit taught by Shiga to control the timing of a plurality of memories based on the deterioration of the reference cell. *See, e.g.,* page 5:8-11 of the instant Office Action. However, the Yamazoe and Shiga references teach different types of memory devices. More specifically, Yamazoe teaches that holes or electrons are injected into a nitride film of a memory transistor. *See, e.g.,* Figures 3 and 4; Col. 1:28-35. In contrast, Shiga teaches a memory cell that has a floating gate in which electrons are trapped. *See, e.g.,* Col. 1:63 to Col. 2:3. Applicant submits that the deterioration of Yamazoe's nitride film device would not provide an indication of the deterioration of Shiga's floating gate

device because these are different types of memory devices. Accordingly, there would be no motivation for one of skill in the art to combine the Yamazoe and Shiga references as proposed by the Office Action. Thus, the Office Action has not provided any evidence as to why one of skill in the art would find the asserted combination obvious as required. Therefore, the Section 103(a) rejection of claims 3-4 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the Section 103(a) rejection of claim 7 because the Office Action has not presented any reason for combining the Shiga and Hirakawa references. This approach is contrary to the requirements of Section 103 and relevant law as discussed above in relation to the Section 103(a) rejection of claims 3 and 4. The Office Action states that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the reference cell in the sense amp since it has been held that rearranging parts of an invention involves only routine skill in the art." *See* page 6:7-9 of the instant Office Action. However, the Office Action fails to present any reason why one of skill in the art would combine Hirakawa's alleged reference cell in a sense amp with the Shiga reference. Accordingly, the Office Action has not provided any evidence as to why one of skill in the art would find the asserted combination obvious as required. Therefore, the Section 103(a) rejection of claim 7 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the Section 103(a) rejection of claims 8-13 because the Office Action has provided no evidence of motivation to combine the Shiga and Yamazoe references as discussed above in relation to the Section 103(a) rejection of claims 3 and 4. Accordingly, the Section 103(a) rejection of claims 8-13 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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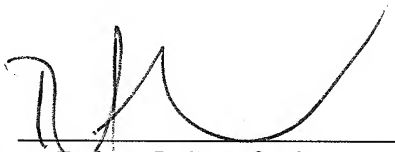
By: 
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